CLAIMS

What is claimed is:

1. A graphics pipeline system for graphics processing, comprising:

(a) a transform module adapted for being coupled to a buffer to receive vertex data therefrom, the transform module being positioned on a single semiconductor platform for transforming the vertex data from object space to screen space;

(b) a lighting module coupled to the transform module and positioned on the same single semiconductor platform as the transform module for performing lighting operations on the vertex data received from the transform module; and

(c) a rasterizer coupled to the lighting module and positioned on the same single semiconductor platform as the transform module and lighting module for rendering the vertex data received from the lighting module.

2. The system as recited in claim 1, wherein the lighting module includes:

(a) a plurality of input buffers adapted for receiving the vertex data;

(b) a multiplication logic unit having a first input coupled to an output of one of the input buffers and a second input coupled to an output of one of the input buffers;

(c) an arithmetic logic unit having a first input coupled to an output of one of the input buffers and a second input coupled to an output of the multiplication logic unit;

(d) a first register unit having an input coupled to the output of the arithmetic logic unit and an output coupled to the first input of the arithmetic logic unit;

(e) a second register unit having an input coupled to the output of the arithmetic logic unit and an output coupled to the first input and the second input of the multiplication logic unit;

(f) a lighting logic unit having a first input coupled to the output of the arithmetic logic unit, a second input coupled to the output of one of the input

buffers, and an output coupled to the first input of the multiplication logic unit; and

(g) a memory coupled to at least one of the inputs of the multiplication logic unit and the output of the arithmetic logic unit.

3. The system as recited in claim 2, wherein an output of one of the input buffers is coupled to an output of the lighting module via a delay.

4. The system as recited in claim 3, wherein the output of the arithmetic logic unit and an output of one of the input buffers are coupled to the output of the lighting module by way of a multiplexer.

5. The system as recited in claim 2, wherein the output of the multiplication logic unit has a feedback loop coupled to the second input thereof.

6. The system as recited in claim 2, wherein the second input of the lighting logic unit is coupled to an output of one of the input buffers via a delay.

7. The system as recited in claim 2, wherein the output of the lighting logic unit is coupled to the first input of the multiplication logic unit via a first-in first-out register unit.

8. The system as recited in claim 2, wherein the output of the lighting logic unit is coupled to the first input of the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

9. The system as recited in claim 1, wherein the transform module includes:

(a) an input buffer adapted for receiving vertex data;

(b) a multiplication logic unit having a first input coupled to an output of the input buffer;

(c) an arithmetic logic unit having a first input coupled to an output of the multiplication logic unit;

(d) a register unit having an input coupled to an output of the arithmetic logic unit;

(e) an inverse logic unit including an input coupled to the output of the arithmetic logic unit or the register unit for performing an inverse or an inverse square root operation;

(f) a conversion module coupled between an output of the inverse logic unit and a second input of the multiplication logic unit, the conversion module adapted to convert scalar vertex data to vector vertex data; and

(g) a memory coupled to the multiplication logic unit and the arithmetic logic unit.

10. The system as recited in claim 9, wherein the memory is coupled to the second input of the multiplication logic unit.

11. The system as recited in claim 9, wherein the memory has a write terminal coupled to the output of the arithmetic logic unit.

12. The system as recited in claim 9, wherein the output of the multiplication logic unit has a feedback loop coupled to the first input thereof.

13. The system as recited in claim 9, wherein the output of the register unit is coupled to the first input of the multiplication logic unit.

14. The system as recited in claim 13, wherein the output of the register unit is coupled to the second input of the multiplication logic unit.

15. The system as recited in claim 9, wherein the output of the arithmetic logic unit has a feedback loop connected to the second input thereof.

16. The system as recited in claim 15, wherein the feedback loop has a delay coupled thereto.

17. The system as recited in claim 1, wherein the rasterizer operates in homogeneous clip space.

18. The system as recited in claim 1, wherein the rasterizer is adapted for receiving a primitive defined by a plurality of vertices each including a W-value; and identifying an area based on the W-values, wherein the area is representative of a portion of a display to be drawn corresponding to the primitive.

19. A graphics pipeline system for graphics processing, comprising:
(a) transform means adapted for being coupled to a buffer to receive vertex data therefrom, the transform means positioned on a single semiconductor platform for transforming the vertex data from object space to screen space;
(c) lighting means positioned on the same single semiconductor platform as the transform means for performing lighting operations on the vertex data received from the transform means; and
(d) rasterizer means positioned on the same single semiconductor platform as the transform means and lighting means for rendering the vertex data received from the lighting means.

20. A method for graphics processing, comprising:
(a) transforming vertex data from object space to screen space;
(b) lighting the vertex data; and
(c) rendering the vertex data, wherein the vertex data is transformed, lighted, and rendered on a single semiconductor platform.

21. The method as recited in claim 20, wherein prior to rendering, the graphics processing further comprises: receiving a primitive defined by a plurality of

vertices each including a W-value; and identifying an area based on the W-values, wherein the area is representative of a portion of a display to be drawn corresponding to the primitive.

22. A graphics pipeline system for graphics processing, comprising:
(a) a lighting module adapted for being coupled to a transform module to receive vertex data therefrom, the lighting module being positioned on a single semiconductor platform for performing lighting operations on the vertex data received from the transform module; and
(b) a rasterizer coupled to the lighting module and positioned on the same single semiconductor platform as the lighting module for rendering the vertex data received from the lighting module.

23. A method for graphics processing, comprising:
(a) lighting vertex data; and
(b) rendering the vertex data, wherein the vertex data is lighted and rendered on a single semiconductor platform.

24. A graphics pipeline system for graphics processing, comprising:
(a) a transform module adapted for being coupled to a buffer to receive vertex data therefrom, the transform module being positioned on a single semiconductor platform for transforming the vertex data from object space to screen space; and
(b) a rasterizer positioned on the same single semiconductor platform as the transform module for rendering the vertex data.

25. A method for graphics processing, comprising:
(a) transforming vertex data from object space to screen space; and
(b) rendering the vertex data, wherein the vertex data is transformed and rendered on a single semiconductor platform.